**Title of the invention:** STRESS AWARE DESIGN FOR INTEGRATED CIRCUITS

<table>
<thead>
<tr>
<th>(54) Title of the invention</th>
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<tbody>
<tr>
<td>(31) Priority Document No</td>
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<td>(57) Abstract:</td>
<td>A method of circuit design involving an integrated circuit (IC) having an interposer can include identifying an active resource implemented within the IC (200 500) within a zone (465 470 535) of the interposer (205 505) exposed to an amount of stress that exceeds a normalized amount of stress on the interposer and selectively assigning an element of the circuit design to be implemented within the IC to the active resource according to a stress aware analysis of the circuit design as implemented within the IC. Another zone (620) is characterized by a substantially normalized stress throughout the other zone.</td>
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**Fig. 4**

No. of Pages : 41 No. of Claims : 11